Addendum to

The Zorro III Bus Specification

# Zorro III Bus Timing

Enhancements, Clarifications, and Other
Zorro III Stuff

*Document Revision 1.0*

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## 1. Bus Loading

The drive requirements of some bus signals have been changed to reflect a more realistic maximum drive. Formerly, there were four drive groups, now there are five. The relaxations consider that no Zorro III backplane will have more than eight slots, and PICs should be able to take advantage of this limitation. Note that most Zorro III bus signals are driven by "F" or

| Signal | Direction | High Level | Low Level |
|---|---|---|---|
| Standard | Loading<br>Driven | +140 uA @ +2.7 VDC<br>+2.5 VDC @ -3.0 mA | -3.2 mA @ +0.4 VDC<br>+0.4 VDC @ +64 mA |
| Clock | Loading | +20 uA @ +2.7 VDC | -1.6 mA @ +0.4 VDC |
| O. C. | Loading<br>Driven | +40 uA @ +2.7 VDC<br>Not Driven | -1.6 mA @ +0.4 VDC<br>+0.4 VDC @ +16 mA |
| Non-bussed | Loading<br>Driven | +40 uA @ +2.7 VDC<br>+2.5 VDC @ -0.4 mA | -1.0 mA @ +0.4 VDC<br>+0.4 VDC @ +4.0 mA |
| Control | Loading<br>Driven | +40 uA @ +2.7 VDC<br>+2.5 VDC @ -1.0 mA | -1.0 mA @ +0.4 VDC<br>+0.4 VDC @ +16 mA |

"FCT" series bus drivers, though in some cases, for some signals or Zorro II boards, "LS" or other CMOS parts may in fact be used. It is possible that many Zorro II cards will work in heavily loaded Zorro III backplanes. Originally, 220/330 Ohm termination was used for Zorro III backplanes on most standard and control lines. Since the A4000, this has been lowered somewhat to 330/440 Ohm termination, and special care has been given to load critical Zorro II signals less, where possible.

### 1.1 Standard Signals

The majority of signals on the bus are in this group. These are bussed signals, driven active on the bus by the appropriate bus master or slave, tri-stated when a change of master, slave, or bus direction takes place. PICs can apply two standard loads to each of these when necessary.

$A_2$-$A_7$ $AD_8$-$AD_{31}$ $SD_0$-$SD_7$ $FC_0$-$FC_2$

### 1.2 Clock Signals

All clock signals on the bus are in this group. Many designs are very sensitive to clock delay, skew, and rise/fall times, so loading on the clock lines must be kept to a minimum. These are bussed signals, actively driven on the backplane by the bus controller, and source terminated with a low value series resistor. PICs can apply one standard load to each of these signals when

necessary. Zorro II cards have the same clock rules, so there should not be clocking problems when using either type of card in a Zorro III backplane. The clock signals, all based on the Zorro II clocking conventions, are:

| | | | |
|---|---|---|---|
| /C3 | CDAC | /C1 | 7M |
| E Clock | | | |

### 1.3 Open Collector SIgnals

Many of the bus signals are shared via open collector or open drain outputs rather than via tri-stated lines. This is, of course, required for some asynchronous shared lines like interrupts, and it works well for other signals as well. The backplane provides pullup resistors for these lines, while PICS simply drive them low to assert them. Some of these signals are actually arbitrated along with the bus cycle, rather than driven asynchronously. For such signals, it is permissible to drive them via tri-stated outputs as long as the drive rules are otherwise met.

| | | | |
|---|---|---|---|
| /OWN | /BGACK | /CINH | /BERR |
| /DTACK | /RESET | /$INT_2$ | /$INT_6$ |
| /HLT | | | |

### 1.4 Non-bussed Signals

The non-bussed, or slot-specific, signals are involved with only one slot on the bus (eg, each slot has its own copy). As a result, the drive requirements are much less for these signals. The backplane provides passive pullups or pulldowns, as required by the specific signal.

| | | | |
|---|---|---|---|
| /$CFGIN_N$ | /$CFGOUT_N$ | /$BR_N$ | /$BG_N$ |
| SenseZ3 | /$SLAVE_N$ | | |

### 1.5 Control Signals

The high-speed control lines are bussed between slots. Loading and routing of these signals is especially critical to the behavior of the entire system. Two loads per signal is possible, though one is recommended if at all possible.

| | | | |
|---|---|---|---|
| /FCS | /CCS | /$DS_0$-/$DS_3$ | /LOCK |
| READ | DOE | /IORST | /BCLR |
| /MTCR | /MTACK | | |

## 2 Multiple Transfer Cycles

Multiple Transfer Cycles, or “burst” mode, is a special mode of the Zorro III bus that allows fast transfers, or subcycles, to be run within one full cycle, Since there is never a change of bus master or bus slave during a multiple transfer cycle, and there is no bus multiplexing, the transfer can run inherently faster than individual full cycles. These cycles have always been

specified for the Zorro III bus, though not implemented in a controller until the A4000. This specification seeks to clear up a number of multiple transfer cycle issues.

### 2.1 Synchronous Burst

The most significant is that there are now two types of Multiple Transfer Cycles supported. The first, *asynchronous burst*, works as always, where the length of a subcycle is determined by the interaction between the bus master's /MTCR strobe and the bus slave's /DTACK. The new cycle type. *synchronous burst*, is basically a simplification of this, in which /DTACK is kept low between subcycles, and timing is based on /MTCR. It was never said that /DTACK couldn't be used this way, but now the resulting timing is specified.

Slaves can choose to implement clocked burst, asynchronous burst, or no burst. Masters must implement both types of burst, or no burst at all. In most designs, synchronous burst is a side-effect asynchronous burst if designed properly.

### 2.2 Pulsed /DTACK

Another simplification is the treatment of /DTACK for asynchronous burst. Formerly, the minimal /DTACK in an asynchronous burst would be 10ns to 15ns in length, based on the minimal /DTACK to /MTCR delay ($T_{OFF}$) of 10ns, plus the slave signal to /MTCR hold time of 0ns to 15ns. It is now required that bus masters supporting burst recognize a /DTACK pulse of 15ns or longer, with no requirement that /DTACK be held beyond /MTCR negated. There is still a requirement that /DTACK be negated properly with respect to /MTCR.

### 2.3 Burst Sizing/Transfer Notes

As mentioned in previous documents, all slave devices must be able to handle a minimum of four longwords of burst without the need to terminate the cycle. While some burs masters may be able to handle this termination, a large class of them cannot. A slave may terminate burst on any cycle past four, which requires any bus master supporting burst with quadlongword transfer restrictions to limits its multiple transfer cycles to four longwords. This is intended to be a compromise between restrictions.

Another consideration for burst is that all transfers much be in whole longword quantities, no byte-lane selection is permitted. Bus masters must still drive the data strobes /$DS_3$-/$DS_0$, but slaves can base all their transfers straight from /MTCR during burst if that's easier to implement. This is designed to eliminate the need for slaves to reconcile the supported data strobe skews during cycles that aren't much longer than this.

### 2.4 Early Byte-Lane Option

There is now an optional early byte lane mode for full cycles. A bus master can, optionally, drive /$DS_3$-/$DS_0$ according to normal address time signal timing. Slaves that don't support this mode see /$DS_N$ at the normal data-time, qualified by DOE. Slaves that do support this mode can latch /$DS_N$ on the falling edge of /FCS. If at least one strobe is valid, the slave gets

## 3 Timing Specification

| No. | Name | Symbol | Min | Max | Note |
|---|---|---|---|---|---|
| 1 | Address-time signal setup to /FCS | TAFS | 15ns | ---- | |
| 2 | Address-time signal hold from /FCS | THAF | 15ns | ---- | |
| 3 | /FCS to slave response signal delay | TSLV | ---- | 25ns | |
| 4 | /FCS to DOS delay | TDOE | 30ns | 100ns | |
| 5 | DOE to /DSN delay | TDS | 10ns | 30ns | |
| 6 | Data setup to /DTACK | TRDS | 0ns | ---- | |
| 6b | Synchronous burst data valid from /MTCR | TRDSb | ---- | 15ns | |
| 7 | /DTACK to /FCS off | TOFF | 10ns | ---- | |
| 8 | Master signal hold from /FCS off | THMC | 0ns | ---- | 1 |
| 8d | Master signal hold from /FCS off, reschedule | THMCr | 0ns | 25ns | |
| 9 | Slave signal hold from /FCS off | THSC | 0ns | 15ns | |
| 10 | Write data setup to /DSN | TWDS | 5ns | ---- | |
| 11 | /FCS to /CCS delay | TCCS | 35ns | 175ns | |
| 12 | /CCS off to /FCS off | TOVL | 40ns | ---- | |
| 13 | Multiple cycle master signal setup to /MTCR | TAMS | 5ns | ---- | |
| 14 | /MTCR pulse high, multiple transfer | TREF | 15ns | ---- | |
| 14q | /MTCR pulse high, quick interrupt | TREFq | 40ns | ---- | |
| 15 | Multiple cycle master signal hold from /MTCR | THAM | 0ns | ---- | |
| 16 | /MTACK setup to /MTCR | TBCD | 10ns | ---- | |
| 17 | Slave signal hold from /MTCR off | THSM | 0ns | 5ns | |
| 17q | Slave signal hold from /MTCR off, quick interrupt | THSMq | 0ns | 15ns | |
| 18 | Poll phase time | TPOL | 30ns | 100ns | |
| 19 | Vector phase start to /DTACK | TVEC | ---- | 100ns | |
| 20 | /DSN group skew | TSKW | ---- | 5ns | |
| 21 | Early data-time signal setup to DOE | TDDS | 10ns | ---- | |
| 22 | Multiple cycle DTACK* pulse width | TDTK | 15ns | ---- | 2 |
| 23 | /MTCR pulse low, multiple transfer | TMTC | 15ns | ---- | |
| 24 | /BRN delay from C7M | THRE | 5ns | 25ns | |
| 25 | /BGN hold from /FCS (reschedule) | THGR | 15ns | 40ns | |
| 26 | /FCS off to new /BGN (reschedule) | TRES | 25ns | ---- | |
| 27 | /BGN to /FCS (acquire) | TACQ | 20ns | 1us | 3 |
| 28 | Mastership timeout from /BGN or /FCS | TBTO | 1us | ---- | |
| 29 | /BRN recycle | TBRC | 3 cyc | ---- | |

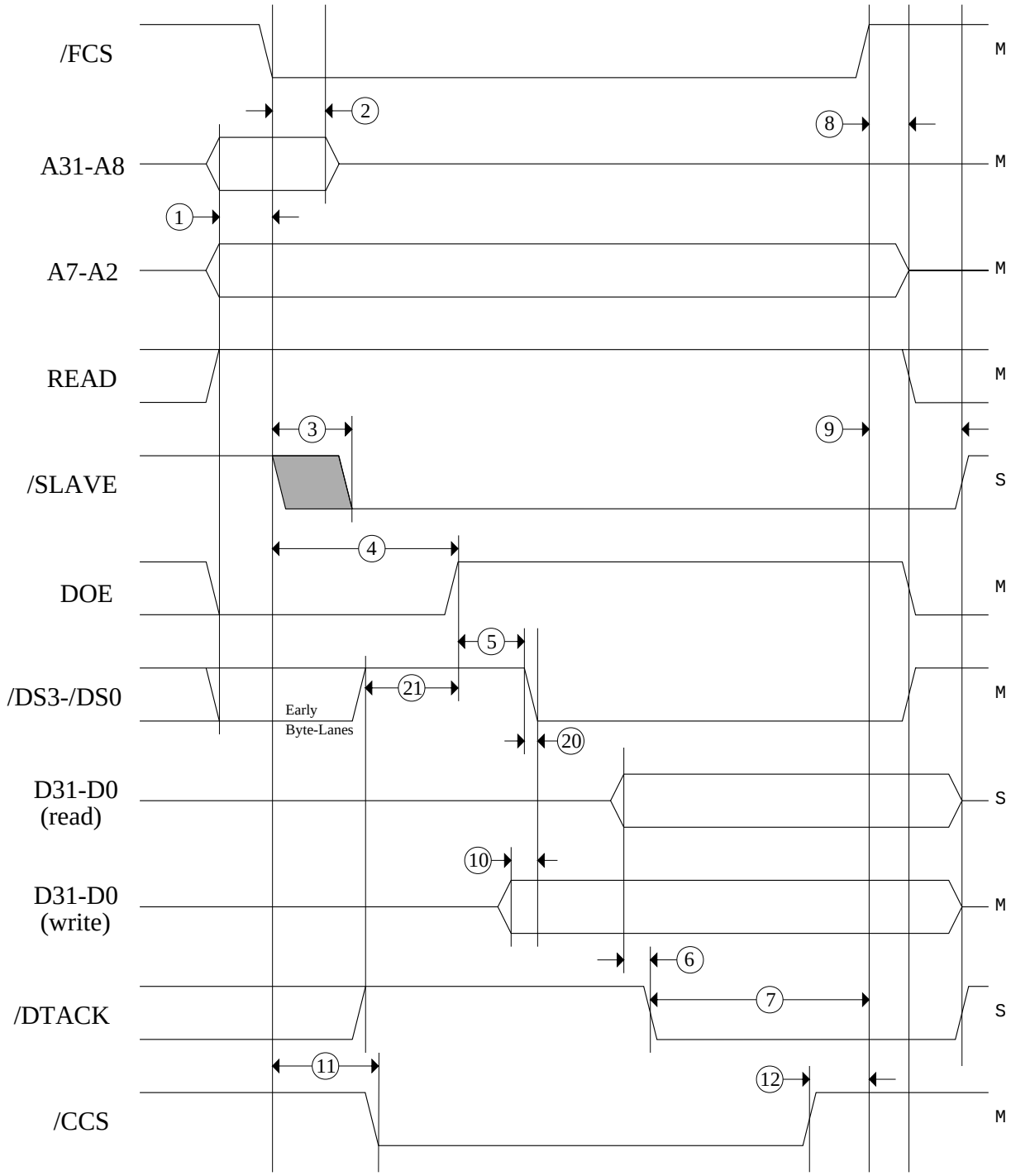
### 3.1 Notes

Note 1: The maximal turnoff time for master-driven signals is only an issue for bus arbitration, given by $T_{HMSd}$. As long as the master holds the bus, its cycle spacing determines this timing.

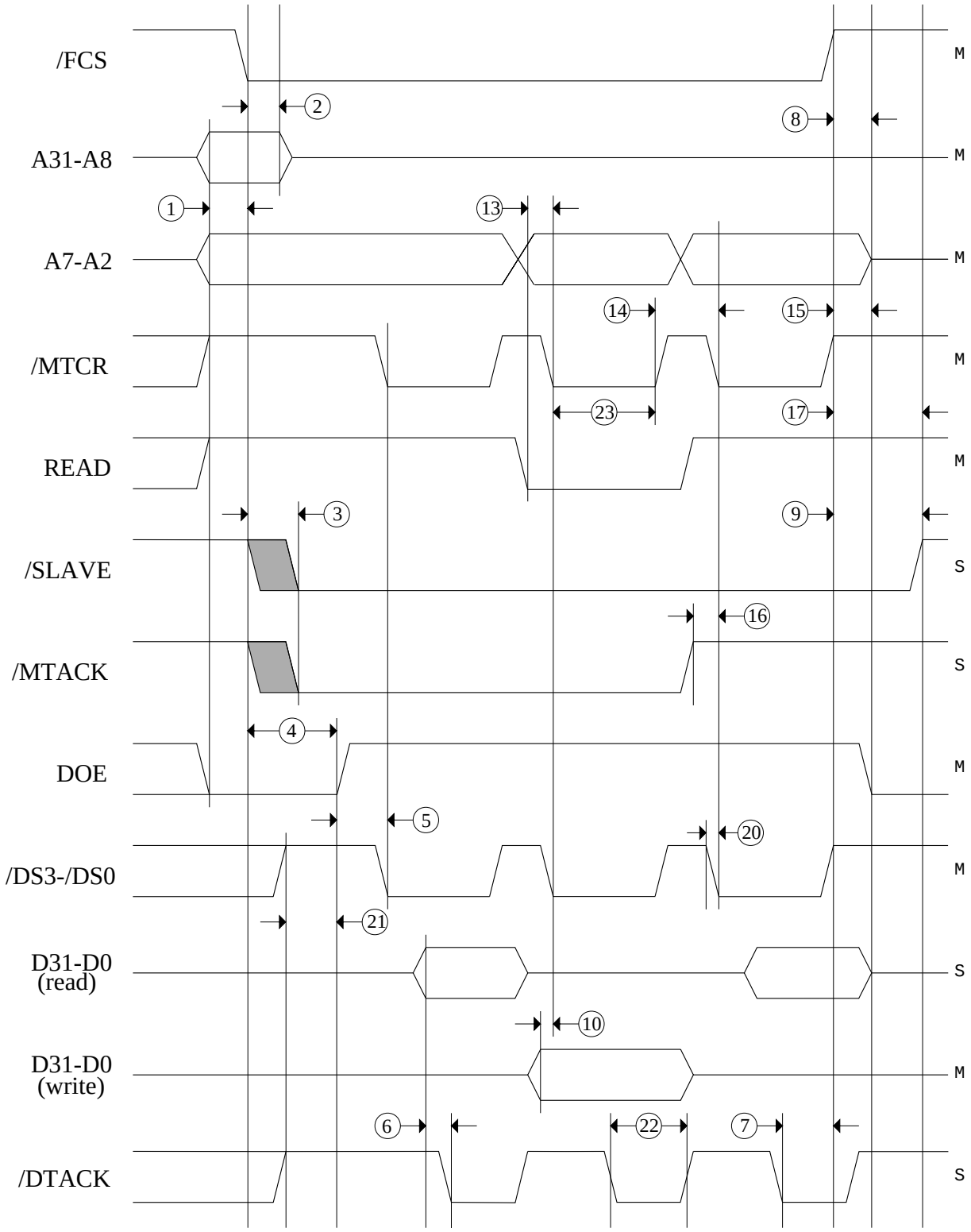
Note 2: The maximal /DTACK pulse width during burst is determined by the burst mode and the required relationship to the /MTCR signal.

Note 3: Failure to acquire the bus results in a mastership timeout.

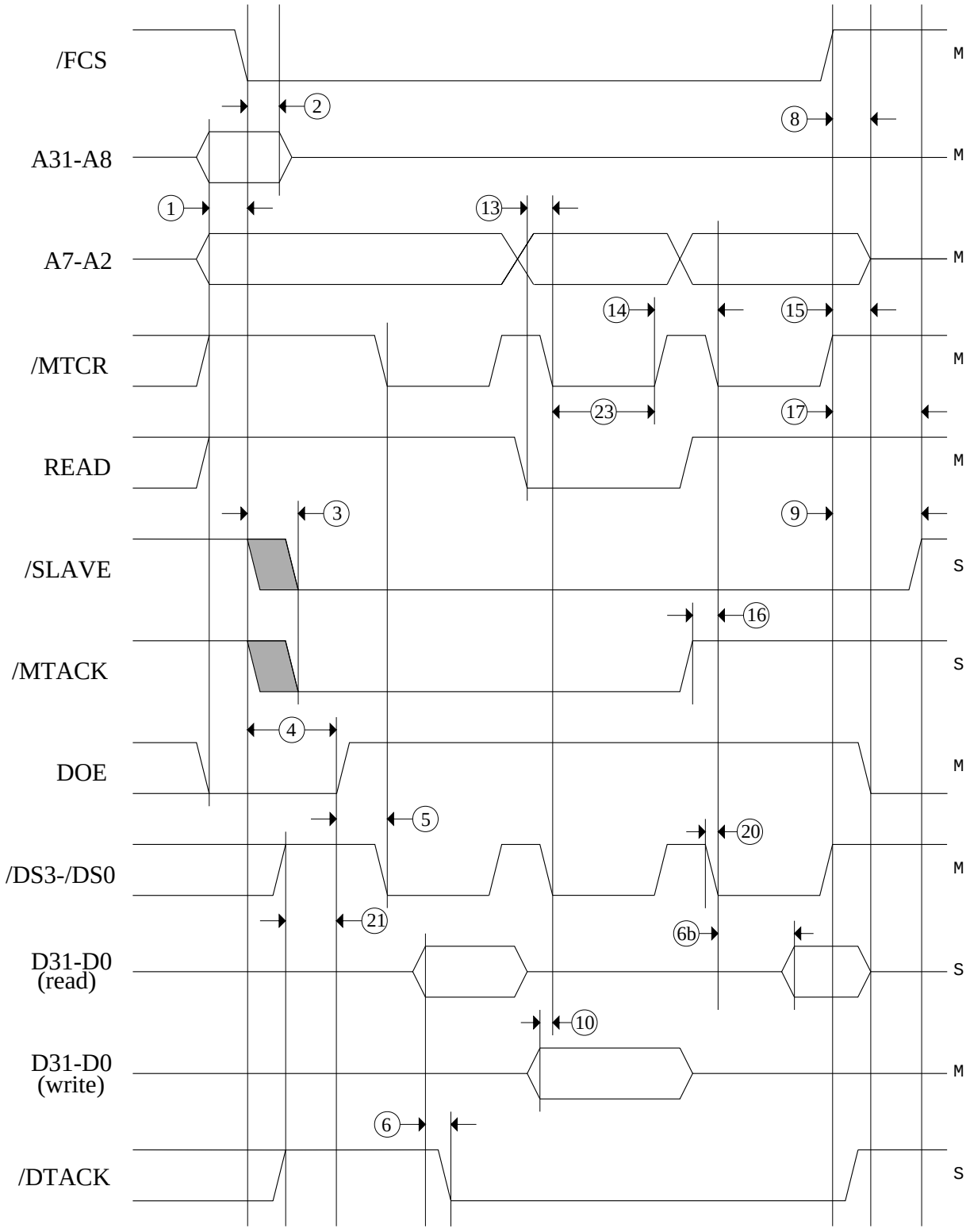
### 3.2 Full Cycle Timing



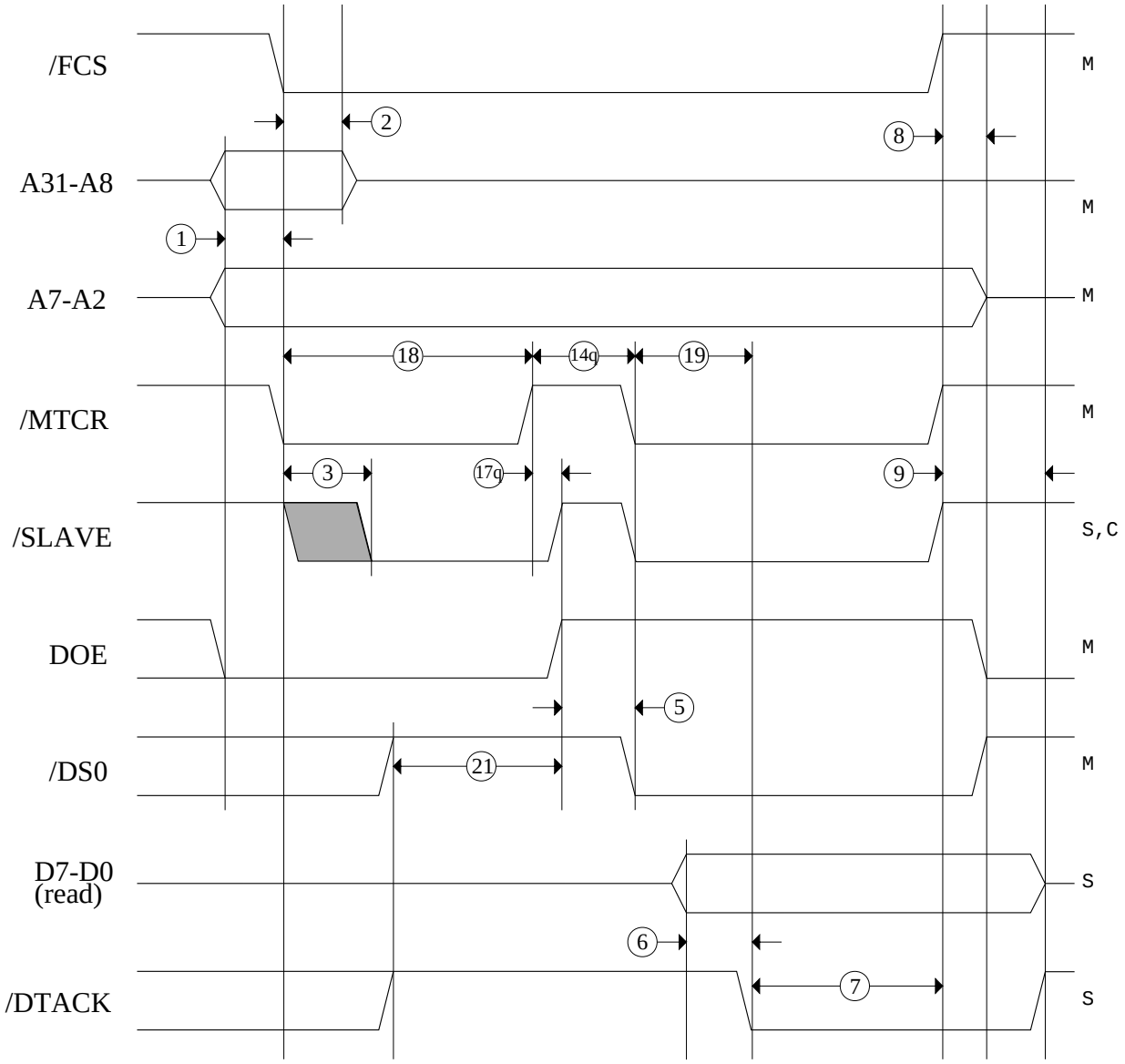
### 3.3 Asynchronous Multiple Transfer Cycle Timing



### 3.4 Synchronous Multiple Transfer Cycle Timing



### 3.5 Quick Interrupt Cycle Timing



### 3.6 Bus Arbitration Timing